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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,872	06/26/2003	John K. Walton	EMC2-143PUS	5270

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EXAMINER	
CASIANO, ANGEL L	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,872	WALTON ET AL.	
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 11* is/are allowed.

6)☒ Claim(s) *1-6,9 and 12-21* is/are rejected.

7)☒ Claim(s) ~~*3,6,7,8,12 and 19*~~ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The present Office action is in response to application dated 26 June 2003.

Claims 1-21 are pending. All claims have been examined.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 9, "138". Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 19 recites the limitation "each one of the first printed circuit boards". However, the claim does not refer previously to "first" printed circuit boards. There is insufficient antecedent basis for this limitation in the claim. Claims 20-21 depend upon claim 19 and are therefore rejected under the same basis.

Claim Objections

6. Claims 3, 5, 12, and 19 are objected to because of the following informalities: "*an* predetermined operating incapability". Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-6, 9, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krontz [US 2004/0003155 A1] in view of Locklear et al. [US 2002/0099875 A1].

Regarding claim 1, Krontz teaches a backplane (Figure 2) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability (see Figure 2, "208", "Slot Speed detector"; Page 1, [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of such electrical contacts being electrically connected to a corresponding one of the plurality of conductors of the backplane; and circuitry connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, "208", "238"; Page 1, [0012]). Krontz et al. also teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, "238"; Page 2, [0026]).

However, Krontz et al. fails to explicitly teach, a *second plurality of printed circuit boards plugged into the backplane selecting an operating characteristic* for electrical

components on the second plurality of printed circuit boards, such selected operating characteristic being *compatible with operating characteristics* of the electrical components on the first plurality of printed circuit boards. As for these limitations, Locklear et al. teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards (see Page 1, [0002]), "an architected method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures in order to obtain a system supporting compatibility with older adapter cards ("printed circuit boards") that do not support the higher data transfer rates, as taught by Locklear et al. (Page 1, [0002]). At the time of the invention, it would have also been obvious that the combination of references provided a system visually indicating configuration problems and solutions for I/O buses, as taught by Locklear et al. (Page 1, [0006]).

As for claim 2, Krontz et al. does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards, as claimed. Locklear et al. teaches a system in which the I/O bus and adapter card "negotiate for the highest supported data transfer rate" (see Page 1, [0002]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Regarding claim 3, Krontz teaches a backplane (Figure 2) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability (see Figure 2, "208", "Slot Speed detector"; Page 1, [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of such electrical contacts being electrically connected to a corresponding one of the plurality of conductors of the backplane. Krontz et al. also teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, "238"; Page 2, [0026]).

However, Krontz et al. fails to explicitly teach, a *second plurality of printed circuit boards plugged into the backplane selecting an operating characteristic* for electrical components on the second plurality of printed circuit boards, such selected operating characteristic being *compatible with operating characteristics* of the electrical components on the first plurality of printed circuit boards. As for these limitations, Locklear et al. teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards (see Page 1, [0002]), "an architected method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 4, Krontz et al. does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards, as claimed. Locklear et al. teaches a system in which the I/O bus and adapter card "negotiate for the highest supported data transfer rate" (see Page 1, [0002]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Regarding claim 5, Krontz teaches a backplane (Figure 2) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of **speed** incapability (see Figure 2, "208", "Slot Speed detector"; Page 1, [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of such electrical contacts being electrically connected to a corresponding one of the plurality of conductors of the backplane; and **circuitry** connected to the plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, "208", "238"; Page 1, [0012]). Krontz et al. also teaches a second plurality of printed circuit boards plugged into a backplane (see Figure 2, "Backplane"). The reference teaches a decoder, responsive to the logic signals on the plurality of conductors (see Figure 2, "238"; Page 2, [0026]) which is to be driven by a clock line (see Page 2, [0027]).

However, Krontz et al. fails to explicitly teach, the *decoders of the second plurality of printed circuit boards coupled to the electric components thereon the one of the plurality of*

clock signals having a rate compatible with operating speeds of the electrical components of the first plurality of printed circuit boards, as claimed. As for these limitations, Locklear et al. teaches a system in which printed circuit boards (see "adapter cards") select an operating characteristic for electric components being compatible with operating characteristics of the first printed circuit boards (see Page 1, [0002]), "an architected method exits whereby the I/O bus and adapter card negotiate for the highest supported data transfer rate").

At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

As for claim 6, the combination of references teaches circuitry as disclosed in claim 5. However, this is not disclosed as providing a wired-NOR configuration. Nonetheless, Examiner notes that a wired-NOR configuration would have been an obvious example for implementing the circuitry as disclosed by the combination of references as exposed above.

As for claim 9, Krontz et al. does not teach selecting the highest speed compatible with the speed capability of the electrical components on the plurality of first printed circuit boards, as claimed. Locklear et al. teaches a system in which the I/O bus and adapter card "negotiate for the highest supported ("compatible") data transfer rate" (see Page 1, [0002]). At the time of the invention, one of ordinary skill in the art would have been motivated to combine the cited disclosures for the reasons stated above.

Regarding claim 18, this corresponds to the method having the steps for implementing the system disclosed in previous claims. The combination of references teaches or suggests all the limitations corresponding to the claimed system and therefore teaches the method implementing it.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 12-17 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Krontz et al. [US 2004/0003155 A1].

Regarding claim 12, Krontz teaches a backplane (Figure 2) having a plurality of conductors; a first plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of an incapability (see Figure 2, "208", "Slot Speed detector"; Page 1, [0010]) of an electrical component on such one of the printed circuit boards (see "Slot"), each one of such electrical contacts being electrically connected to a corresponding one of the plurality of conductors of the backplane; and circuitry connected to the

plurality of conductors for converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals on the plurality of conductors (see Figure 2, "208", "238"; Page 1, [0012]).

As for claim 13, Krontz et al. explicitly discloses the signals as identifying the current operating speed of the expansion slots (see Page 2, [0024]).

Regarding claim 14, Krontz teaches a backplane system (Figure 2) having a plurality of conductors; a plurality of printed circuit boards plugged into the backplane (see Figure 2, 200), each one of the first printed circuit boards having a plurality of electrical contacts, each one of the electrical contacts providing an indication of the current operating speeds (see Figure 2, "208", "Slot Speed detector"; Page 1, [0010]) of an electrical component on such one of the printed circuit boards (see "Slot").

Regarding claim 15, this corresponds to the method having the steps for implementing the system disclosed in previous claims. Krontz et al. teaches all the limitations corresponding to the claimed system and therefore teaches the method implementing it. Furthermore, Krontz et al. teaches interrupting start-up of the system upon detection of operating incompatibility (see Page 4, [0037]; Figure 5).

As for claims 16 and 17, the Krontz et al. reference teaches incompatibility in operating speed and protocol (see Page 3, [0034]; "slot speed indicators 402-408 are used to indicate both

the current operating speed of the expansion slot 400 and whether the adapter card in the expansion slot is a PCI or PCI-X adapter card").

Regarding claim 19, this corresponds to the method having the steps for implementing the system disclosed in previous claims. Krontz et al. teaches all the limitations corresponding to the claimed system and therefore teaches the method implementing it. Furthermore, Krontz et al. teaches converting the operating incapability indications provided by the plurality of printed circuit boards into logic signals for the plurality of printed circuit boards (see Page 3, [0029]).

As for claims 20 and 21, the Krontz et al. reference teaches incompatibility in operating speed and protocol (see Page 3, [0034]; "slot speed indicators 402-408 are used to indicate both the current operating speed of the expansion slot 400 and whether the adapter card in the expansion slot is a PCI or PCI-X adapter card").

Allowable Subject Matter

12. Claims 10-11 are allowed.

13. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: As for the cited claims (7,8,10,11), the prior art fails to teach, alone or in combination, a first plurality of printed circuit boards having a plurality of *electrical contacts*, each of the electrical

contacts providing an indication of a predetermined speed incapability, wherein ***each*** *one of the plurality of contacts is* ***connected*** *to a* ***ground potential*** *when such contact provides an* ***indication of operating speed incapability****; otherwise such contact is* ***open circuited*** (emphasis added).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Brown et al. [US 20030126334 A1] teaches a computer system which "includes a backplane having sockets into which system and peripheral boards may be inserted. The sockets are coupled together by a backplane bus that includes a bus capability line. Each board preferably includes a voting circuit that, when enabled, limits the voltage on the capability signal line to no more than a predetermined voltage that is indicative of the capability of the board. The voltage on the capability signal line will thus be determined by the board having the lowest voltage limit. The clock source for the bus can then be set to the clock rate indicated by the voltage on the capability signal line. Zener diodes are preferably used to carry out the voting operation, and may be disabled after the voting operation is complete".
- Vianna et al. [US 20020160743 A1] teaches a backplane that "generally accepts APMs via slot connectors in order to connect them to other parts of the system. Motherboards on modern personal computers can be considered to be a general

equivalent to backplanes in communication systems. Backplanes also typically distribute power to each module connected thereto".

- Miller et al. [US 6,820,156 B1] teaches the "motherboard of a computer system comprises light emitting diodes associated to each slot of a PCI bus to indicate whether an adapter card inserted into the slot is limiting the transmission speed on the bus associated to the respective slot".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L. Casiano whose telephone number is 571-272-4142. The examiner can normally be reached on 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alc
17 October 2005

KIM HUYNH
PRIMARY EXAMINER
10/17/05